

### REMARKS

Applicants have amended claims 1 and 25 and added claim 29.

Claim 25 has been rejected under 35 USC 102(b) as anticipated by U.S. Patent No. 6,124,736 (Yamashita). Applicants respectfully traverse this rejection.

In the Action, the Examiner repeats, virtually words for words, the same argument against claim 25 as in the previous Action dated May 6, 2003, and maintains his assertion that FIG. 3 of Yamashita teaches the claimed switching circuit device. At page 9 of the Action, the Examiner acknowledges applicants' argument in the previous amendment filed August 1, 2003 that the signals inputted through Yamashita's leads are not outputted from the output leads O, O' of Yamashita. However, the Examiner fails to respond to this argument directly. Instead, the Examiner recreates portions of the claim which include the expression "electrically in contact with," changes the expression to read "directly electrically in contact with," and states in essence that claims 1 and 25 do not distinguish over Yamashita because the claims do not comply with the change proposed by the Examiner.

Applicants do not fully understand what the Examiner meant by "directly electrically in contact with" and assume that the expression means "electrically in direct contact with." Persons of ordinary skill in the art would have understood that A being electrically in direct contact with B means that there is no high impedance element in the electric path between A and B. Based on this understanding, applicants have amended the claims to recite "electrically in direct contact with." As a result, claim 25 recites, for example, a first common output terminal pad being electrically in direct contact with the source electrode or the drain electrode of the first transistor. Yamashita's circuit on the other hand has the gate insulating film of the MOSFET, which provides a high impedance, in the electric path between the lead O, which the Examiner equates

to the claimed common output terminal pad, and the source or drain of Yamashita's FET.

Accordingly, Yamashita's circuit does not have the common output terminal which is electrically in direct contact with the source electrode or the drain electrode.

In response to applicants' argument in the previous amendment that Yamashita describes no terminal pad structure at all, the Examiner repeats the same argument that the end portion of Yamashita's leads O, O', I0, I0', I1, I1' in the circuit block shown in FIG. 3 are the claimed terminal pads. The text portion of Yamashita describes no terminal pad structures. The only evidence the Examiner provides as teaching the claimed pads is the circuit diagram, FIG. 3, which does not show any pad structure as claimed and described in the specification. Without providing evidence that persons of ordinary skill in the art would have understood the end portions of the leads to be the claimed terminal pads, this rejection fails.

Yamashita does not teach or suggest the claimed invention. Thus, the rejection of claim 25 under 35 USC 102(b) on Yamashita should be withdrawn

Claims 1-5, 7, 8, 10-12 and 26 have been rejected under 35 USC 103(a) as unpatentable over Yamashita in view of Background of the Invention section of the specification. Applicants respectfully traverse this rejection.

Claim 1 as amended recites "electrically in direct contact with," the same limitation as claim 25, which Yamashita does not teach or suggest, as explained above.

In addition, in response to applicants' argument that the Examiner failed to provide evidence that persons of ordinary skill in the art would have been motivated to combine Yamashita and the Background section to arrive at the claimed invention, the Examiner repeats the same argument at page 5 of the Action:

Therefore, it would have been obvious to one of ordinary skill in the art to form the Yamashita et al.'s device having a semiconductor switching circuit

device formed on a substrate and each of transistors of the switching circuit having a source electrode, a gate electrode and a drain electrode which are formed on a channel layer such as taught by APA because such structure is conventional in the art for forming the field effect transistor.

In trying to maintain this argument, the Examiner incorrectly cites *In re Fine* in manner that takes the court's comment out of the context. *Fine* stated, including the portion relied upon by the Examiner, that:

The PTO has the burden under section 103 to establish a *prima facie* case of obviousness. ... It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the reference. ... This it has not done. The Board points to nothing in the cited references, either alone or combination, suggesting or teaching Fine's invention.

837 F.2d at 1074, 5 USPQ2d at 1603-04 (citation omitted). In *Fine*, the Examiner stated, "Substitution of detectors to measure any component of interest is well within the skill of the art." *Id.* at 1073, at 1601. As cited above, the Court determined that such a statement does not create a *prima facie* case of obviousness.

Applicants submit that the Examiner's statement that the claimed structure is conventional is the very type of statement that the Court refused to accept as evidence of the obviousness of the combination in *Fine*. Furthermore, the Examiner's statement does not rebut applicants' argument regarding the combination of Yamashita and the Background section. Rather, his logic is that the claimed structure is in his opinion conventional and thus obvious. This is testament to a finding that the invention would have been obvious simply because the Examiner says so.

As applicants explained in the previous amendment, Yamashita's circuit is a digital logic circuit, and the switching circuit described in the Background section is an analog circuit, i.e., handling CDMA or GPS signals. Those two types of circuits belong to two distinctively

different arts. For example, the methods of energizing the two circuits are different and not compatible to each other, as explained in the previous amendment. The Examiner must provide evidence that persons of ordinary skill in the art would have been motivated to combine Yamashita and the Background section to arrive at the claimed invention despite the difficulty explained above. Based on *Fine* and *Lee*, as explained in the previous amendment, the Examiner's statement that the claimed structure is conventional is not enough to establish a *prima facie* case of obviousness. Thus, this rejection fails.

Yamashita and the Background section together do not show the claimed invention as a whole. Thus, the rejection of claims 1-5, 7, 8, 10-12 and 26 under 35 USC 103(a) should be withdrawn.

Claims 27 and 28 have been rejected under 35 USC 103(a) as unpatentable over Yamashita. Applicants respectfully traverse this rejection.

The Examiner admits that Yamashita does not teach or suggest the claimed two single pole double throw switches, and states that it is obvious to arrive at the claimed structure because such a structure is conventional. As explained above, the Examiner's statement fails to constitute objective evidence, which *Fine* and *Lee* require, that persons of ordinary skill in the art would have been motivated to modify Yamashita's circuit, which does not include single pole double throw switches, to include single pole double throw switches. Thus, the rejection of claims 27 and 28 should be withdrawn.

Applicants have added claim 29. The claimed feature that the four input terminal pads are configured to receive two pairs of balanced analog signals and the two common output terminal pads are configured to output one of the two pairs of balanced analog signals received by the four input terminal pads finds support, for example, at page 19, line 20 - page 20, line 4,

of the specification. Applicants point out that the persons of ordinary skill in the art would have known that a CDMA signal or a GPS signal is an analog signal.

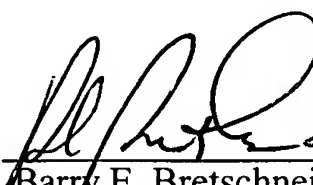
In light of the above, a Notice of Allowance is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952**, referencing Docket No. 492322002400.

Respectfully submitted,

Dated: April 19, 2004

By:

  
Barry E. Bretschneider  
Registration No. 28,055

Morrison & Foerster LLP  
1650 Tysons Boulevard, Suite 300  
McLean, VA 22102-3915  
Telephone: (703) 760-7743  
Facsimile: (703) 760-7777